Claims

Having thus described the invention, what is claimed is:

1. A semiconductor carrier structure comprising:

a semiconductor substrate comprising a substrate material having a first coefficient of thermal expansion and a first elastic modulus;

at least one through-via in said semiconductor substrate, wherein each of said through-vias is filled with a conductive structure having a second coefficient of thermal expansion which is less than or substantially the same as the first coefficient of thermal expansion and a second elastic modulus which is less than or equal to the first elastic modulus.

2. The semiconductor carrier structure of Claim 1 wherein said conductive structure comprises a metal-ceramic composite.

3. The semiconductor carrier structure of Claim 2 wherein said metal-ceramic composite comprises a metallic conductive material with a CTE-matched ceramic.

4. The semiconductor carrier structure of Claim 3 wherein said CTE-matched ceramic is selected from the group consisting of cordierite, silicate-based glasses, glass ceramic, alumina, mullite, fosterite, sapphire.

5. The semiconductor carrier structure of Claim 2 wherein said metal ceramic composite is formed from a metallic coated powder suspension.

6. The semiconductor carrier structure of Claim 5 wherein said metallic coated powder suspension is selected from the group consisting of borosilicate glasses, CSVP, Cu-coated W, Ta, SiC, SiO2, Ni/Ti alloy, Si, zirconium-tungsten oxide, silver coated W, Au coated W, Au coated over copper shell over W core, Au/Ti/Cu/W, Au/Cr/Ni/W, Au/Ti/Ni/Mo, Au/Ti/Cu/Si, and Au/Cr/Cu/ZrW2O8.

7. The semiconductor carrier structure of Claim 1 wherein said each conductive structure comprises a first conductive via material disposed in annular shape along the sidewalls of said through-via and having a core structure comprising a second via material.

8. The semiconductor carrier structure of Claim 7 wherein said second via material comprises an insulating material.

9. The semiconductor carrier structure of Claim 7 wherein said second via material comprises a conducting material.

10. The semiconductor carrier structure of Claim 7 wherein said second via material comprises said substrate material.

11. The semiconductor carrier structure of Claim 7 wherein said second via material is selected from the group consisting of polyimide, thermid, KJ, photosensitive polyimide, SiLK, or other high-temperature polymer.

12. The semiconductor carrier structure of Claim 7 wherein said second via material comprises a material having a third coefficient of thermal expansion which is less than or about equal to said first coefficient of thermal expansion.

13. The semiconductor carrier structure of Claim 7 wherein said second via material comprises silicate glass.

14. The semiconductor carrier structure of Claim 7 wherein said second via material comprises of silica or a silicate glass-filled high temperature polymer.

15. The semiconductor carrier structure of Claim 7 wherein said second via material comprises a sealed void filled with vacuum or a gas.

16. The semiconductor carrier structure of Claim 2 wherein said substrate material is selected from the group consisting of silicon, silicate glass, alumina, mullite, fosterite, sapphire, gallium arsenide, gallium phosphide, aluminum nitride, glass ceramic, silicon carbide, beryllium oxide, or a glass fiber-impregnated high temperature polymer.

17. The semiconductor carrier structure of Claim 1 wherein said conductive structure compress a low CTE metal-core metal powder.

18. The semiconductor carrier structure of Claim 1 wherein said conductive structure comprises a low CTE insulating-core, metal coated powder.

19. The semiconductor carrier structure of Claim 1 wherein said conductive structure comprises a mixture of particles having different core and shell materials.

20. The semiconductor carrier structure of Claim 1 wherein the top surface of said conductive structure comprises one of an impermeable solid metal or an insulating cap.

21. The semiconductor carrier structure of Claim 20 where said insulating cap includes a spin-applied high-temperature polymer core.

22. The semiconductor carrier structure of Claim 20 where the insulating cap includes a lamination of high temperature polymer film.

23. The semiconductor carrier structure of Claim 1 further comprising an insulating layer disposed along the sidewalls of each of said through-vias between said substrate and said conductive structure.

24. The semiconductor carrier structure of Claim 1 further comprising an insulating layer on the bottom surface of the substrate adjacent to said at least one through-via.

25. The semiconductor carrier structure of Claim 1 wherein said second coefficient of thermal expansion is less than about 8 ppm/°C, and wherein said second elastic modulus is less than or equal to 170GPa.

26. A method for fabricating a semiconductor carrier structure in a semiconductor substrate comprising substrate material having a first coefficient of thermal expansion and first elastic modulus comprising the steps of:

etching a plurality of blind via holes from the top surface of said semiconductor substrate to a depth which is less than the thickness of said semiconductor substrate;

providing an insulating layer on the exposed surfaces of said blind via holes;

creating a conductive structure in each of said plurality of blind via holes, said conductive structure having a second coefficient of thermal expansion which is less than or substantially the same as said first coefficient of thermal expansion and a second elastic modulus which is less than or equal to the first elastic modulus.

27. The method of Claim 26 further comprising creating at least one of integrated circuits, wiring, and components on at least one of the top and the bottom surface.

28. The method of Claim 26 further comprising electrically contacting said integrated circuit, wiring, or components to said through-vias.

29. The method of Claim 26 further comprising exposing the bottom of each of said conductive structures by removing substrate material from the bottom of said substrate structure and removing said insulating layer at the bottom of said blind via holes.

30. The method of Claim 26 wherein etching of vias is a high-rate process which includes alternating etching and deposition steps performed with substrate temperatures between 0°C and -100°C and more preferably -50°C.

31. The method of Claim 29 whereby said exposing comprises a mechanical backside grind and polish process.

32. The method of Claim 29 wherein said exposing comprises the steps of:

removing the bulk of the backside silicon by grinding and polishing; and

recessing the silicon surface below the via bottoms by selective wet etching.

34. The method of Claim 33 further comprising passivating the exposed silicon by conformal insulator deposition.

35. The method of Claim 34 further comprising exposing the conductive surface of the via bottom by CMP.

36. The method of Claim 26 further comprising planarizing the top of said semiconductor carrier structure to remove any conductive material disposed on the top surface of the substrate.

37. The method of Claim 26 wherein said creating a conductive structure comprises disposing metal-ceramic in said through-vias.

38. The method of Claim 37 wherein said disposing metal-ceramic comprises the steps of:

filling said blind via holes with a highly loaded metal-ceramic suspension/paste; and

heating said structure to provide continuous conductive networks and impart mechanical integrity.

39. The method of Claim 26 wherein said substrate is silicon and wherein said providing of an insulating layer comprises exposing said substrate to passivating to provide insulating material along the sidewalls of each of said through-vias between said substrate and said conductive structure.

40. The method of Claim 26 wherein said creating a conductive structure comprises the steps of:

providing a core structure comprising an inner via material; and

disposing a conductive via material in annular shape about said core structure.

41. The method of Claim 26 wherein said creating a conductive structure comprises the steps of:

disposing a first conductive via material in annular shape over said insulated layer, to provide an annular conductive ring with a remaining inner via volume; and

filling said remaining inner via volume with a second via material having a coefficient of thermal expansion which is less than said first coefficient of thermal expansion.

42. The method of Claim 26 wherein said etching comprises etching an annular ring for said blind vias to provide a core structure of said substrate material and wherein said creating a conductive structure comprises disposing conductive material in said annular ring.

43. The method of Claim 26 wherein creating a conductive structure comprises the steps of:

disposing a conductive via material in annular shape along the insulated surfaces of each of said blind via holes; and

burnishing conductive via surface material at the surface of said blind via holes in conductive contact with said conductive via material, whereby air/gas/vacuum/ambient is sealed within said via hole.